Notice of Allowability		Application No.			
		10/720,123			
		Examiner	Art Unit		
	,	taka B. Talasad	0.400		
		John P. Trimmings	2138		
The MAILING DATE of the All claims being allowable, PROSECUT herewith (or previously mailed), a Notice NOTICE OF ALLOWABILITY IS NOT A of the Office or upon petition by the app	ION ON THE MERITS IS e of Allowance (PTOL-85) A GRANT OF PATENT RI	(OR REMAINS) CLOSED in or other appropriate commu GHTS. This application is si	nication will be mailed in due	ed course. <b>THIS</b>	
1. X This communication is responsive to the amendment and RCE dated 2/28/2007.					
2. The allowed claim(s) is/are <u>1-16.</u>	<u>18-23, renumbered as 1-2</u>	<u>22</u> .			
3. ☑ Acknowledgment is made of a c a) ☑ All b) ☐ Some* c) ☐ 1. ☑ Certified copies of th	None of the:		or (f).		
2. Certified copies of the priority documents have been received in Application No					
3. Copies of the certified copies of the priority documents have been received in this national stage application from the					
International Bureau (PCT Rule 17.2(a)).					
* Certified copies not received:					
Applicant has THREE MONTHS FRO noted below. Failure to timely comply THIS THREE-MONTH PERIOD IS NO	will result in ABANDONM		a reply complying with the req	uirements	
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.					
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.					
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached					
1)  hereto or 2)  to Paper No./Mail Date					
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date					
Identifying indicia such as the applica each sheet. Replacement sheet(s) sho				back) of	
6. DEPOSIT OF and/or INFORM attached Examiner's comment re				ote the	
Attachment(s)					
1. Notice of References Cited (PTO-892)		5. Notice of Inf	formal Patent Application		
2.  Notice of Draftperson's Patent Drawing Review (PTO-948)			6. Interview Summary (PTO-413), Paper No./Mail Date 20070326.		
3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date			7. ⊠ Examiner's Amendment/Comment		
4. Examiner's Comment Regarding F	Requirement for Deposit	8. 🛛 Examiner's S	Statement of Reasons for Allo	wance	
of Biological Material	40	9.			
	ER	John P Trimmings	Juni		
			Examiner	•	

# **DETAILED ACTION**

This office action is in response to the applicant's amendment and RCE dated 2/28/2007.

The applicant has amended claims 1, 8-9, 15-16 and 19.

The applicant has canceled claims 17 and 24-25.

Claims 1-16 and 18-23 are pending.

## Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/28/2007 has been entered.

#### **EXAMINER'S AMENDMENT**

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

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Authorization for this examiner's amendment was given in a telephone interview with Linus Park on 3/21/2007. The examiner amends the claims 1, 8, 15 and 16 as follows:

1. (Currently Amended) A speed binning test circuit, comprising:

a plurality of circuit groups arranged along a boundary of a chip circuit, each circuit group including a different number of unit delay circuits with respect to each other; and

a plurality of pads, each pad disposed between two adjacent circuit groups of the plurality of circuit groups, wherein each of the pad pads is connected to at least one output terminal of one of the two adjacent circuit groups and also connected to at least one input terminal of the other of the two adjacent circuit groups; and

wherein the circuit groups comprise combinational circuits.

8. (Currently Amended) A semiconductor device, comprising:

a plurality of signal input/output pins;

a core circuit including logic that receives or outputs a signal via the plurality of signal input/output pins; and

a speed binning test circuit including:

a plurality of circuit groups, each circuit group including a different number of unit delay circuits with respect to each other arranged in a chain structure along the boundary of the core circuit,—and

a plurality of pads, each pad disposed between two adjacent circuit groups of the plurality of circuit groups, wherein each of the-pad pads is connected to at least one output terminal of one of the two adjacent circuit groups and also connected to at least one input terminal of the other of the two adjacent circuit groups; and

wherein the circuit groups comprise combinational circuits.

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15. (Currently Amended) A speed binning test method, comprising:

delaying test signals through a plurality of successively connected circuit groups, each of the plurality of successively connected circuit groups including different number of unit delay circuits with respect to each other, that forms a chain structure on a chip,—and

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monitoring on-chip-variations to determine total signal delay time through the chain structure at a plurality of pads, each pad disposed between two adjacent circuit groups of the plurality of circuit groups, wherein each of the <u>pad pads</u> is connected to at least one output terminal of one of the two adjacent circuit groups and also connected to at least one input terminal of the other of the two adjacent circuit groups; and

wherein the circuit groups comprise combinational circuits.

16. (Currently Amended) The method of claim 15, further comprising receiving the test signals from the unit delay circuit groups on the chip via a plurality of signal input/output pins.

## Response to Arguments

3. In view of the applicant's amendments to the claims, and further in view of the examiner's amendments to the claims, all prior rejections to the claims are herein withdrawn.

## Allowable Subject Matter

4. Claims 1-16 and 18-23 are allowed. The following is an examiner's statement of reasons for allowance: The referenced art of Inoshita and Patrie disclose an apparatus

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and method of speed binning a circuit wherein the circuit comprises a plurality of delay circuit groups arranged on the periphery of the circuit, and comprising a different number of delay circuits each, each group connected to the next through a pad interconnect. But the references have failed to further disclose or suggest the unique feature claimed by the applicant, wherein the circuit groups comprise combinational circuits. Therefore, claims 1-16 and 18-23 are allowed, and are renumbered as claims 1-22.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings

Examiner Art Unit 2138

jpt

GUY LAMARRE PRIMARY EXAMINER